

Appl. No. 10/618,012  
Amdt. Dated January 16, 2006  
Reply to Office Action of October 18, 2005

**AMENDMENTS TO THE SPECIFICATION:**

On pages 8 - 9 of the Specification, please amend the last full paragraph of page 8 to read:

**Marked-up version:**

An example of each pixel 20 in the pixel section 12 is shown in Fig. 12 2. The pixel 20 includes a pixel transistor 21 as an active element (e.g., a thin film transistor (TFT)), a liquid crystal cell 22 having a pixel electrode connected to the drain electrode of the TFT 21, and a storage capacitor 23 having one electrode connected to the drain electrode of the TFT 21. The liquid crystal cell 22 represents a liquid crystal capacitance generated between the pixel electrode and a common electrode formed opposing the pixel electrode.

**Clean version:**

An example of each pixel 20 in the pixel section 12 is shown in Fig. 2. The pixel 20 includes a pixel transistor 21 as an active element (e.g., a thin film transistor (TFT)), a liquid crystal cell 22 having a pixel electrode connected to the drain electrode of the TFT 21, and a storage capacitor 23 having one electrode connected to the drain electrode of the TFT 21. The liquid crystal cell 22 represents a liquid crystal capacitance generated between the pixel electrode and a common electrode formed opposing the pixel electrode.

On page 12 of the Specification, please amend the second full paragraph to read:

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Marked-up version:

In Fig. 3, a shift register  $31_{n-1}$  in the stage  $n-1$ , a shift register  $31_n$  in the stage  $n$ , and a shift register  $31_{n+1}$  in the stage  $n+1$  are cascade-connected. An Output pulse from each of the shift registers  $31_{n-1}$ ,  $31_n$ , and  $31_{n+1}$  is supplied as one input to each of AND gates  $32_{n-1}$ ,  $32_n$ , and  $32_{n+1}$ . Each of the AND gates  $32_{n-1}$ ,  $32_n$ , and  $32_{n+1}$  is supplied with an output pulse as the other input from each of next-stage shift registers  $32_{n-1}$ ,  $32_n$ , and  $32_{n+1}$ . An output pulse from each of the AND gates  $32_{n-1}$ ,  $32_n$ , and  $32_{n+1}$  is supplied as one input to each of the AND gates  $33_{n-1}$ ,  $33_n$ , and  $33_{n+1}$ .

Clean version:

In Fig. 3, a shift register  $31_{n-1}$  in the stage  $n-1$ , a shift register  $31_n$  in the stage  $n$ , and a shift register  $31_{n+1}$  in the stage  $n+1$  are cascade-connected. An Output pulse from each of the shift registers  $31_{n-1}$ ,  $31_n$ , and  $31_{n+1}$  is supplied as one input to each of AND gates  $32_{n-1}$ ,  $32_n$ , and  $32_{n+1}$ . Each of the AND gates  $32_{n-1}$ ,  $32_n$ , and  $32_{n+1}$  is supplied with an output pulse as the other input from each of next-stage shift registers  $31_n$ ,  $31_{n+1}$ , and  $31_{n+2}$ . An output pulse from each of the AND gates  $32_{n-1}$ ,  $32_n$ , and  $32_{n+1}$  is supplied as one input to each of the AND gates  $33_{n-1}$ ,  $33_n$ , and  $33_{n+1}$ .

On pages 12 - 13 of the Specification, please amend the last full paragraph of page 12 to read:

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Marked-up version:

Each of the AND gates 33n-1, 33n, and 33n+1 receives, as the other ~~output~~ input, an enable pulse ENB for permitting row selection. An output pulse from each of the AND gates 33n-1, 33n, and 33n+1 is supplied as one input to each of OR gates 34n-1, 34n, and 34n+1. Each of the OR gates 34n-1, 34n, and 34n+1 receives, as the other input, the control signal C1 output when the power-off state is detected by the power-off detection circuit 18. An output pulse from each of the OR gates 34n-1, 34n, and 34n+1 is supplied as a scanning pulse (gate pulse) to each of gate lines 24n-1, 24n, and 24n+1 through each of buffers 35n-1, 35n, and 35n+1.

Clean version:

Each of the AND gates 33n-1, 33n, and 33n+1 receives, as the other input, an enable pulse ENB for permitting row selection. An output pulse from each of the AND gates 33n-1, 33n, and 33n+1 is supplied as one input to each of OR gates 34n-1, 34n, and 34n+1. Each of the OR gates 34n-1, 34n, and 34n+1 receives, as the other input, the control signal C1 output when the power-off state is detected by the power-off detection circuit 18. An output pulse from each of the OR gates 34n-1, 34n, and 34n+1 is supplied as a scanning pulse (gate pulse) to each of gate lines 24n-1, 24n, and 24n+1 through each of buffers 35n-1, 35n, and 35n+1.